Remarks/Arguments

Claims 1-27 are pending in this application. Claims 1, 12, and 24 have been amended. Is it respectfully submitted that no new matter has been added.

Claims 1, 2, 5, 9, 10, and 24-27 are rejected under 35 USC § 103(a) as being unpatentable over Leupers *et al.*, "Generation of Interpretive and Compiled Instruction Set Simulators" ("Leupers") in view of U.S. Patent No. 5,781,758 to Morley ("Morley"), further in view of U.S. Patent No. 7,107,580 to Zemach *et al.* ("Zemach").

Claims 3, 4, 6-8, and 11 are rejected under 35 USC § 103(a) as being unpatentable over Leupers in view of Morley, further in view of Zemach, and further in view of U.S. Pub. No. 2005/0102493 by DeWitt, Jr. *et al* ("DeWitt").

Claims 12-16, 18, 18, 22, and 23 are rejected under 35 USC § 103(a) as being unpatentable over U.S. Patent No. 6,477,683 to Killian *et al.* ("Killian"), in view of DeWitt, further in view of Leupers, further in view of Morley, further in view of Zemach.

Claim 17 is rejected under 35 USC § 103(a) as being unpatentable over Killian, in view of DeWitt, further in view of Leupers, further in view of Morley, further in view of Zemach, further in view of U.S. Pub. No. 2003/0217248 by Nohl *et al.* ("Nohl").

Claims 20 and 21 are rejected under 35 USC § 103(a) as being unpatentable over Killian, in view of DeWitt, further in view of Leupers, further in view of Morley, further in view of Zemach, further in view of U.S. Pub. No. 2005/0160402 by Wang *et al.* ("Wang").

I. Rejections under 35 USC §103

A. Claims 1, 2, 5, 9, 10, and 24-27 are rejected under 35 USC § 103(a) as being unpatentable over Leupers in view of Morley, further in view of Zemach. Applicants respectfully traverse the rejections and submit that Claims 1, 2,5, 9, 10 and 24-27 are patentable under 35 U.S.C. §103(a) over Leupers in view of Morley, further in view of Zemach for at least the following reasons.

Claim 1 recites:

> each template configured to implement a functionality of an instruction contained within an instruction class, the instruction class describing a set of instructions of the instruction set architecture having a common behavior;

> reducing a set of original instructions of a target application program to a subset of the plurality of templates...**optimizing the subset of templates by compiling the subset of templates into a decoded program**.

Claim 1, emphasis added. As the Examiner acknowledged, Leupers does not provide such a teaching, and specifically does not disclose:

> wherein the template is associated with an instruction class that describes a set of instructions of the instruction set architecture having a common behavior, and wherein the original instruction is contained in the instruction class.

10/18/2011 Office Action, p. 3.

As with Leupers, Morley does not provide such a teaching. Instead, Morley describes dynamically generating semantic routines on demand during emulation rather than statically storing all routines in the body of a software emulation system. Morley, col. 2, ll. 22-26. An application program consists of commands that are designed for the instruction set of an emulated processor, and a set of instructions in the native code which emulates instructions in emulated code is referred to as a semantic routine. Morley, col. 3, ll. 20-48. For the specific emulated instruction that corresponds to a semantic routine that is statically stored in emulator code, a dispatch table entry comprises a pointer to a stored semantic routine. Morley, col. 2, .ll 20-37. In other words, Morley describes replacing pointers to each routine of an emulation system to semantic routines. Morley does not teach:

> each template configured to implement a functionality of an instruction contained within an instruction class, the instruction class describing a set of instructions of the instruction set architecture having a common behavior; reducing a set of original instructions of a target application program to a subset of the plurality of templates...**optimizing the subset of templates by compiling the subset of templates into a decoded program**.

Claim 1, emphasis added. Zemach does not provide such a teaching either. Zemach describes translating a sequence of target instructions on a host machine using a simulator. Zemach, col. 1, ll. 35-40. The simulator includes a binary translator to translate the target code into host machine code. Zemach, col. 1, ll. 41-48. The binary translator translates a sequence of target instructions and stores the translated code in a translation cache.

Zemach, col. 1, ll. 56-62. Once translated, a block of translated code may be executed on the host processor a number of times from the translated cache. *Id.* Zemach does not teach:

> each template configured to implement a functionality of an instruction contained within an instruction class, the instruction class describing a set of instructions of the instruction set architecture having a common behavior; reducing a set of original instructions of a target application program to a subset of the plurality of templates...**optimizing the subset of templates by compiling the subset of templates into a decoded program.**

Claim 1, emphasis added. Because neither Leupers, Morley, nor Zemach, alone or in combination, teach or suggest all of the features of Claim 1, Applicants respectfully submit that Claim 1, and Claims 2-11 that depend from Claim 1, are patentable under 35 U.S.C §103(a) over Leupers, Morley, and Zemach.

Claim 24 recites substantially similar limitations as recited in Claim 1, including:

> each template configured to implement a functionality of an instruction contained within an instruction class, the instruction class describing a set of instructions of the instruction set architecture having a common behavior; reducing a set of original instructions of a target application program to a subset of the plurality of templates...**optimizing the subset of templates by compiling the subset of templates into a decoded program**.

Claim 24, emphasis added. For the reasons discussed above regarding the rejection of Claim 1, neither Leupers, Morley, nor Zemach, alone or in combination, teach or suggest all of the features of Claim 24. Therefore, Applicants respectfully submit that Claim 24, and Claims 25-27 that depend from Claim 24 are patentable under 35 U.S.C. §103(a) over Leupers, Morley, and Zemach.

B. Claims 3, 4, 6-8, and 11 are rejected under 35 USC § 103(a) as being unpatentable over Leupers in view of Morley, further in view of Zemach, and further in view of DeWitt. Applicants respectfully traverse the rejections and submit that Claims 3, 4, 6-8, and 11 are patentable under 35 U.S.C. §103(a) over Leupers in view of Morley, further in view of Zemach, and further in view of DeWitt for at least the following reasons.

Claims 3, 4, 6-8, and 11 depend from Claim 1, and Claim 1 recites:

> each template configured to implement a functionality of an instruction contained within an instruction class, the instruction class describing a set of instructions of the instruction set architecture having a common behavior; reducing a set of original instructions of a target application program to a subset of the plurality of templates...**optimizing the subset of templates by compiling the subset of templates into a decoded program**.

Claim 1, emphasis added. For the reasons discussed above regarding the rejection of Claim 1, neither Leupers, Morley, nor Zemach provide such a teaching. DeWitt does not provide such a teaching either. Instead, DeWitt describes obtaining performance data in a data processing system. DeWitt, ¶[0003]. As a processor processes instructions, an instruction cache determines which instructions are associated with performance indicators. DeWitt, ¶[0074]. Signals associated with performance indicators are sent to a performance monitor unit. *Id.* DeWitt does not teach:

> each template configured to implement a functionality of an instruction contained within an instruction class, the instruction class describing a set of instructions of the instruction set architecture having a common behavior; reducing a set of original instructions of a target application program to a subset of the plurality of templates...**optimizing the subset of templates by compiling the subset of templates into a decoded program**.

Claim 1, emphasis added. Because neither Leupers, Morley, Zemach, nor DeWitt, alone or in combination, teach or suggest all of the features of Claim 1, Applicants respectfully submit that Claims 3, 4, 6-8, and 11 that depend from Claim 1 are patentable under 35 U.S.C. §103(a) over Leupers, Morley, Zemach, and DeWitt.

C. Claims 12-16, 18, 18, 22, and 23 are rejected under 35 USC § 103(a) as being unpatentable over Killian, in view of DeWitt, further in view of Leupers, further in view of Morley, further in view of Zemach. Applicants respectfully traverse the rejections and submit that Claims 12-16, 18, 18, 22, and 23 are patentable under 35 U.S.C. §103(a) over Killian, in view of DeWitt, further in view of Leupers, further in view of Morley, and further in view of Zemach for at least the following reasons.

Claim 12 recites:

> each template configured to implement a functionality of an instruction contained within an instruction class, the instruction class describing a set of instructions of the instruction set architecture having a common behavior; reducing a set of original instructions of a target application program to a subset of the plurality of templates...**optimizing the subset of templates by compiling the subset of templates into a decoded program**.

Claim 12, emphasis added. For the reasons discussed above, neither DeWitt, Leupers, Morley, nor Zemach provide such a teaching. Killian does not provide such a teaching either. Instead, Killian describes automatically configuring a processor by generating a description of a hardware implementation of the processor and a set of software development tools for programming the processor. Killian, col. 6, ll. 32-37. A configured definition of a target instruction set is developed from a standardized language. Killian, col. 6, ll. 50-65. Instructions are defined into a class, and each instruction in a class has the same format and operand usage. Killian, col. 16, ll. 14-20. An instruction semantic statement describes the behavior of one or more instructions. Killian, col. 16, ll. 40-50. Killian does not teach:

> each template configured to implement a functionality of an instruction contained within an instruction class, the instruction class describing a set of instructions of the instruction set architecture having a common behavior; reducing a set of original instructions of a target application program to a subset of the plurality of templates...**optimizing the subset of templates by compiling the subset of templates into a decoded program**.

Claim 12, emphasis added. Because neither Killian,DeWitt, Leupers, Morley, Zemach, nor DeWitt, alone or in combination, teach or suggest all of the features of Claim 12, Applicants respectfully submit that Claim 12, and Claims 13-23 that depend from Claim 12 are patentable under 35 U.S.C. §103(a) over Killian, DeWitt, Leupers, Morley, and Zemach.

D. Claim 17 is rejected under 35 USC § 103(a) as being unpatentable over Killian, in view of DeWitt, further in view of Leupers, further in view of Morley, further in view of Zemach, further in view of Nohl. Applicants respectfully traverse the rejection and submit that Claim 17 is patentable under 35 U.S.C. §103(a) over Killian, in view of DeWitt,

further in view of Leupers, further in view of Morley, further in view of Zemach, and further in view of Nohl for at least the following reasons.

Claim 17 depends from Claim 12, and Claim 12 recites:

> each template configured to implement a functionality of an instruction contained within an instruction class, the instruction class describing a set of instructions of the instruction set architecture having a common behavior; reducing a set of original instructions of a target application program to a subset of the plurality of templates...**optimizing the subset of templates by compiling the subset of templates into a decoded program**.

Claim 12, emphasis added. For the reasons discussed above, neither Killian, DeWitt, Leupers, Morley, nor Zemach provide such a teaching. Nohl does not provide such a teaching either. Instead, Nohl describes simulating a program by accessing a table of compiled instructions. Nohl, ¶[0019]. If compiled data for an instruction is not stored in the table, the instruction is compiled and data is stored in the table for it. *Id.* By storing compiled data in the table, the instruction need not be compiled again if the instruction is re-executed. *Id.* Compiled data includes information suitable for the simulator to execute the instruction. Norl, ¶[0039]. Nohl does not teach:

> each template configured to implement a functionality of an instruction contained within an instruction class, the instruction class describing a set of instructions of the instruction set architecture having a common behavior; reducing a set of original instructions of a target application program to a subset of the plurality of templates...**optimizing the subset of templates by compiling the subset of templates into a decoded program**.

Claim 12, emphasis added. Because neither Killian, DeWitt, Leupers, Morley, Zemach, nor Nohl, alone or in combination, teach or suggest all of the features of Claim 12, Applicants respectfully submit that Claim 17 that depends from Claim 12 is patentable under 35 U.S.C. §103(a) over Killian, DeWitt, Leupers, Morley, Zemach, and Nohl.

E. Claims 20 and 21 are rejected under 35 USC § 103(a) as being unpatentable over Killian, in view of DeWitt, further in view of Leupers, further in view of Morley, further in view of Zemach, further in view of Wang. Applicants respectfully traverse the rejection and submit that Claims 20 and 21 are patentable under 35 U.S.C. §103(a) over Killian, in view

of DeWitt, further in view of Leupers, further in view of Morley, further in view of Zemach, and further in view of Wang for at least the following reasons.

Claims 20 and 21 depend from Claim 12, and Claim 12 recites:

> each template configured to implement a functionality of an instruction contained within an instruction class, the instruction class describing a set of instructions of the instruction set architecture having a common behavior; reducing a set of original instructions of a target application program to a subset of the plurality of templates...**optimizing the subset of templates by compiling the subset of templates into a decoded program**.

Claim 12, emphasis added. For the reasons discussed above, neither Killian, DeWitt, Leupers, Morley, nor Zemach provide such a teaching. Wang does not provide such a teaching either. Instead, Wang describes adding advanced instructions to a microprocessor. Wang, ¶[0008]. A processor generated using instruction extensions includes an instruction fetch unit to decode the advanced instructions added. Wang, ¶[0031]. Operation classes associate opcodes with operands, and opcodes determine the behavior of an instruction including the opcode. Wang, ¶[0102]. Opcodes are used to determine hardware and software associated with an execution unit for the opcode. *Id.* Wang does not teach:

> each template configured to implement a functionality of an instruction contained within an instruction class, the instruction class describing a set of instructions of the instruction set architecture having a common behavior; reducing a set of original instructions of a target application program to a subset of the plurality of templates...**optimizing the subset of templates by compiling the subset of templates into a decoded program**.

Claim 12, emphasis added. Because neither Killian, DeWitt, Leupers, Morley, Zemach, nor Wang, alone or in combination, teach or suggest all of the features of Claim 12, Applicants respectfully submit that Claims 20 and 21 that depend from Claim 12 are patentable under 35 U.S.C. §103(a) over Killian, DeWitt, Leupers, Morley, Zemach, and Wang.

Thus, the cited combination of references does not disclose, nor suggest, the novel features of the inventions claimed in claims 1-27.

II. Conclusion

Prompt and favorable action on the merits of the claims is earnestly solicited. Should the Examiner have any questions or comments, the undersigned can be reached at (949) 567-6700.

The Commissioner is authorized to charge any fee which may be required in connection with this Amendment to deposit account No. 15-0665.

Respectfully submitted,
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